FIG. 1A (PRIOR ART)

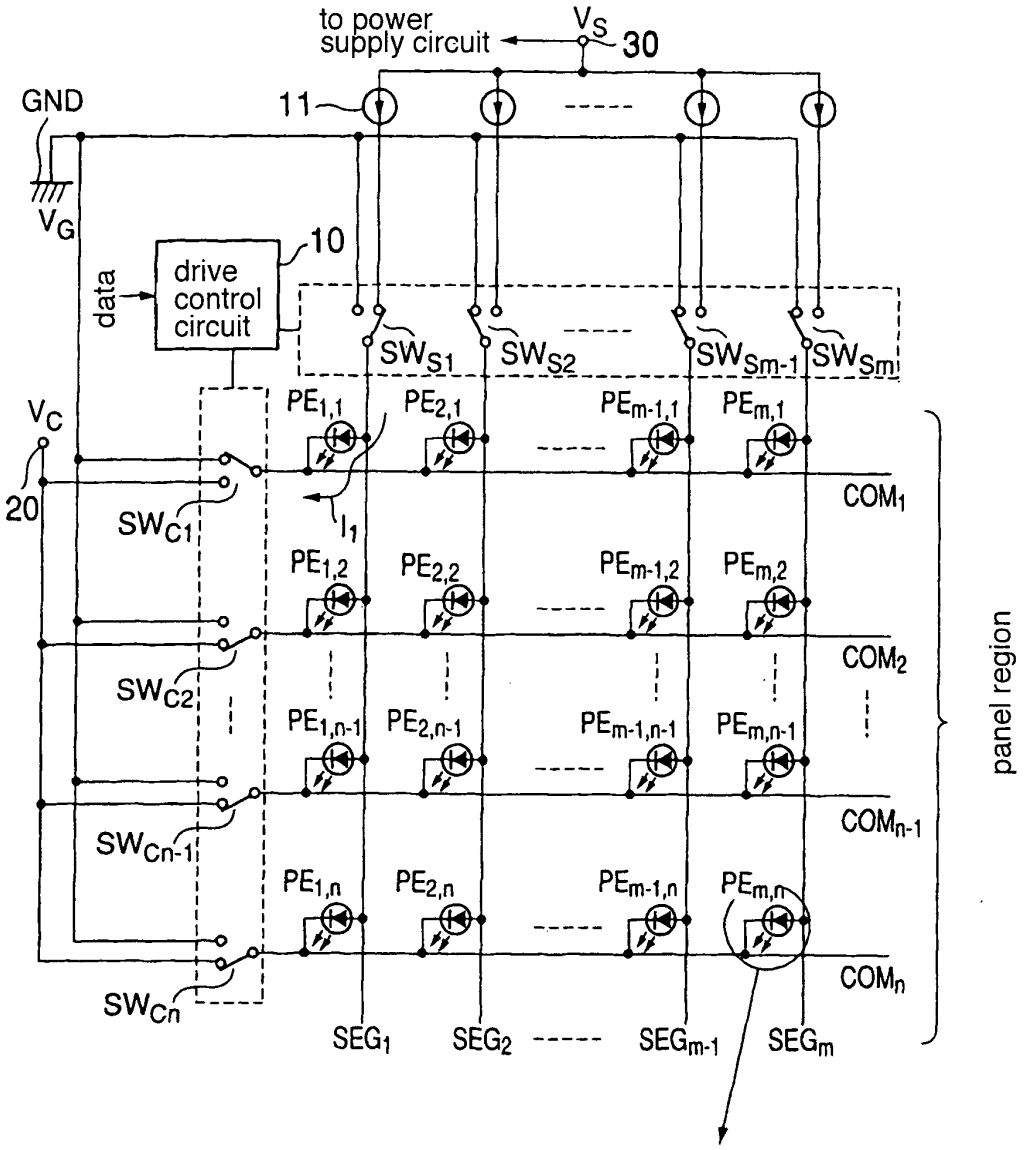

FIG. 1B (PRIOR ART)

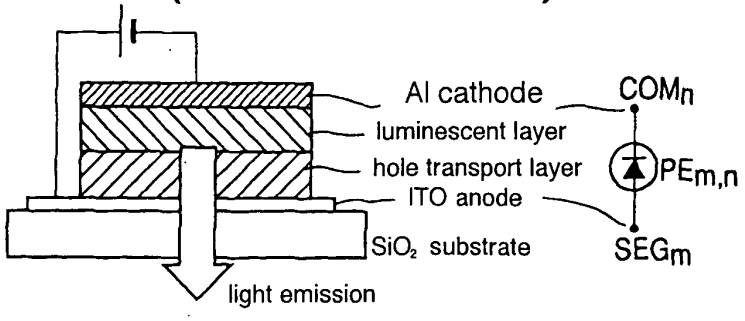

FIG. 2

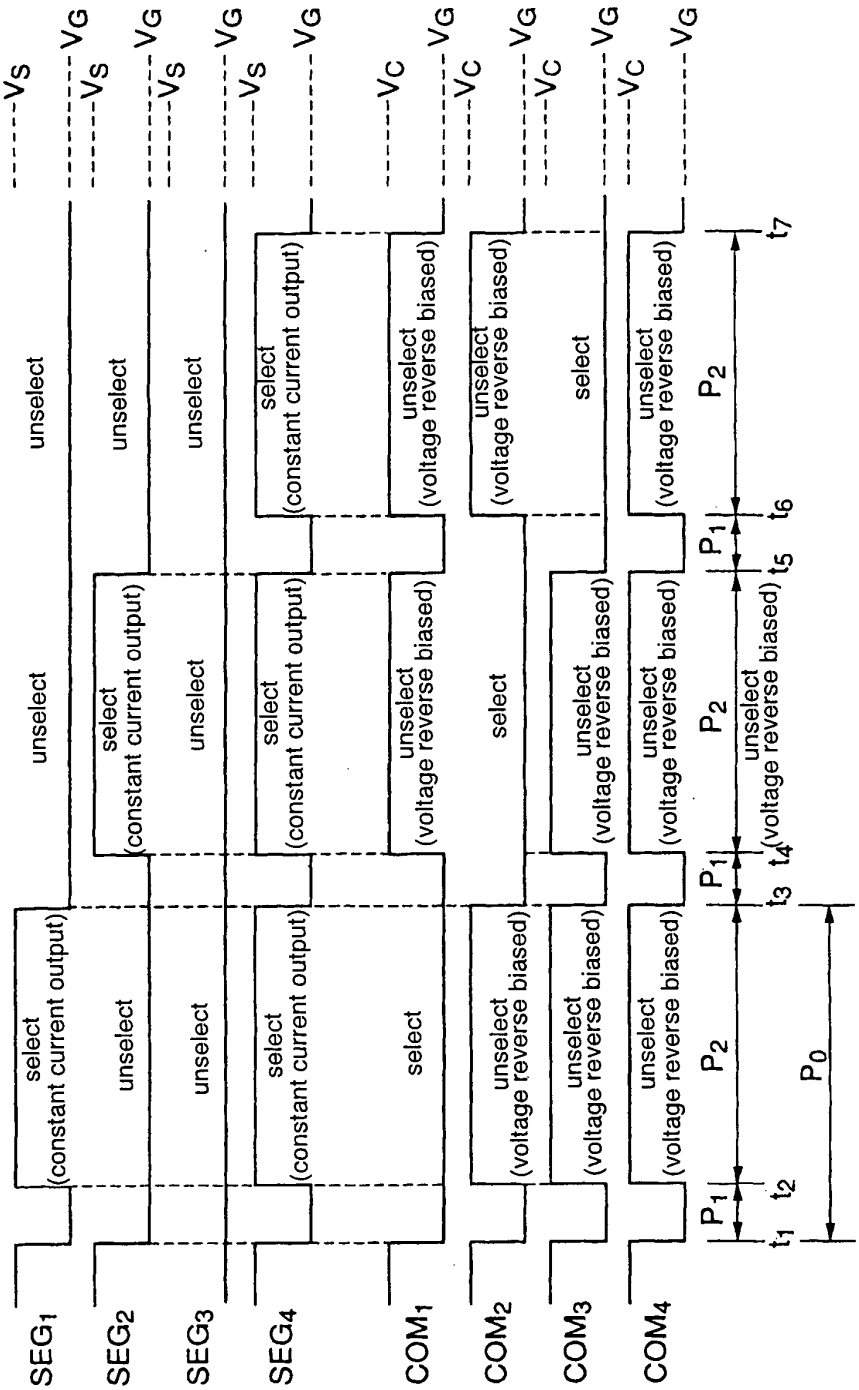
SEG1
SEG2
SEG3
SEG4
COM1
COM2
COM3
COM4
select (constant current output)
unselect (voltage reverse biased)
unselect
VS
VC
VG
P0
P1
P2
t1
t2
t3
t4
t5
t6
t7

FIG. 3 (PRIOR ART)

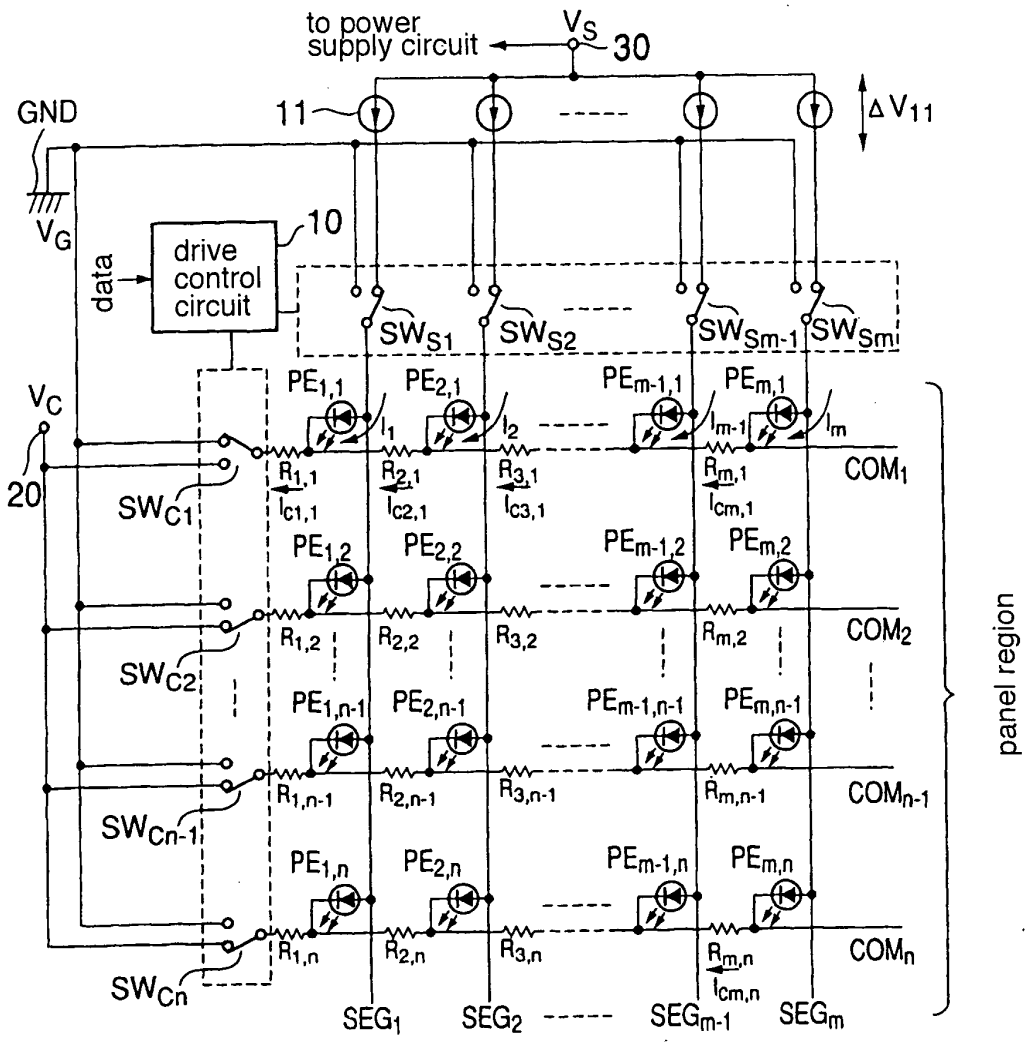

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FIG. 4

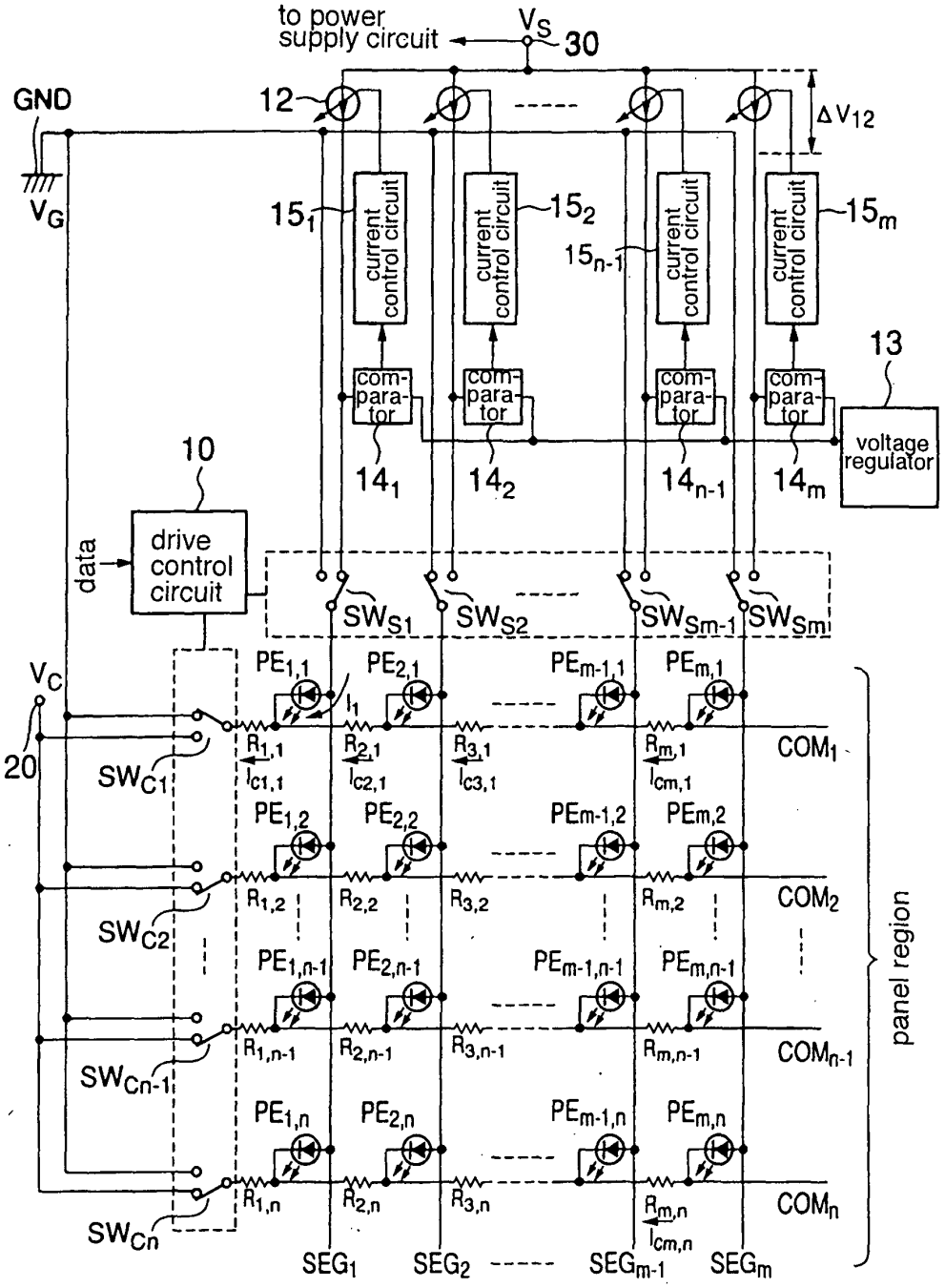

FIG. 5

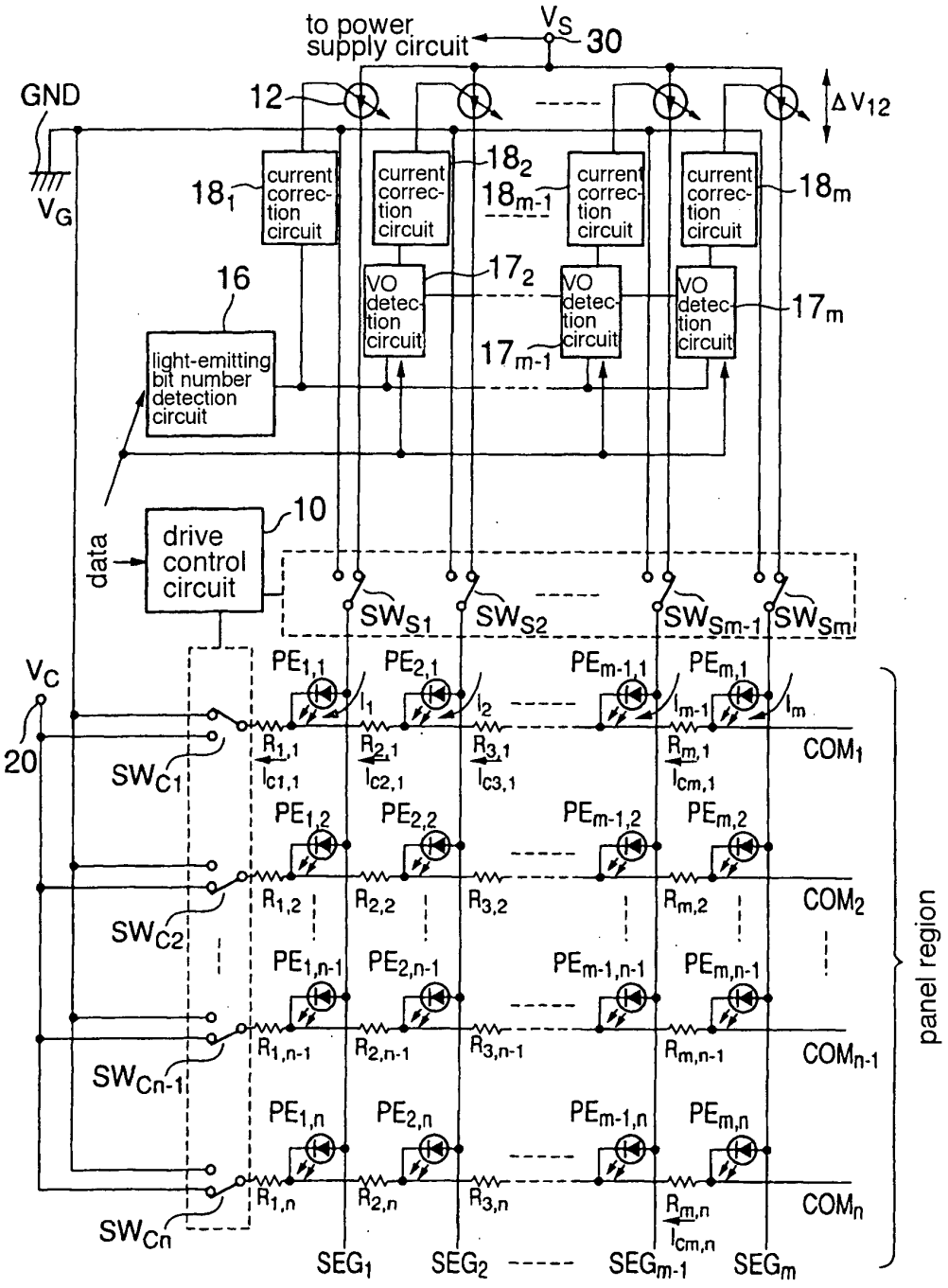
to power supply circuit
V_S
30
GND
V_G
12
ΔV_{12}
18_1
18_2
18_{m-1}
18_m
current correction circuit
16
17_2
17_{m-1}
17_m
VO detection circuit
light-emitting bit number detection circuit
data
drive control circuit
10
SW_{S1}
SW_{S2}
SW_{Sm-1}
SW_{Sm}
V_C
20
SW_{C1}
SW_{C2}
SW_{Cn-1}
SW_{Cn}
$PE_{1,1}$ $PE_{2,1}$ $PE_{m-1,1}$ $PE_{m,1}$
$PE_{1,2}$ $PE_{2,2}$ $PE_{m-1,2}$ $PE_{m,2}$
$PE_{1,n-1}$ $PE_{2,n-1}$ $PE_{m-1,n-1}$ $PE_{m,n-1}$
$PE_{1,n}$ $PE_{2,n}$ $PE_{m-1,n}$ $PE_{m,n}$
I_1 I_2 I_{m-1} I_m
$R_{1,1}$ $R_{2,1}$ $R_{3,1}$ $R_{m,1}$
$I_{c1,1}$ $I_{c2,1}$ $I_{c3,1}$ $I_{cm,1}$
$R_{1,2}$ $R_{2,2}$ $R_{3,2}$ $R_{m,2}$
$R_{1,n-1}$ $R_{2,n-1}$ $R_{3,n-1}$ $R_{m,n-1}$
$R_{1,n}$ $R_{2,n}$ $R_{3,n}$ $R_{m,n}$
$I_{cm,n}$
COM_1
COM_2
COM_{n-1}
COM_n
panel region
SEG_1 SEG_2 SEG_{m-1} SEG_m

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FIG. 6

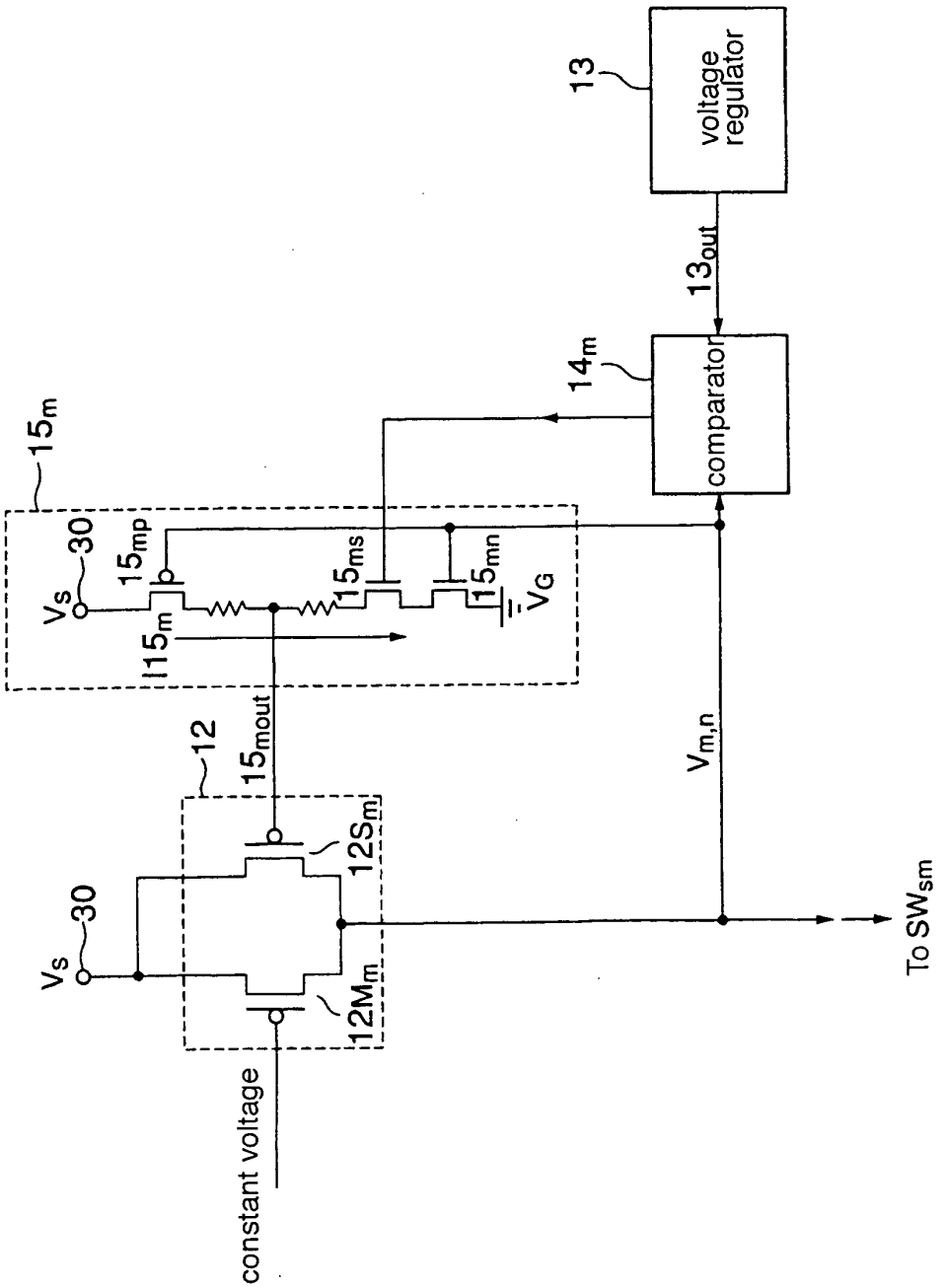

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FIG. 7